a packet distributor unit configured to receive data packets and matching classification information for the packets, and to input each of the packets to one of the plurality of cryptography processing engines;

wherein the combination of said distributor unit and plurality of cryptography engines is configured to provide for cryptographic processing of a plurality of the packets from a given packet flow in parallel while maintaining per flow packet order.

an internal bus that connects the central processing unit, the system memory, the network interface unit, and the cryptography acceleration chip.

[24] 23. The device of claim [23] 22, wherein the internal bus is a high speed switching matrix.

REMARKS

These amendments are made to correct typographical errors in the claims as originally filed. No new matter is added.

Should the Examiner have any questions regarding this Preliminary Amendment, please do not hesitate to contact the undersigned.

Respectfully submitted,
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